DISPLAY LINE DRIVERS AND METHOD FOR SIGNAL PROPAGATION DELAY COMPENSATION

Background of the Invention

1. Field of the Invention: The present invention relates generally to row and column drivers of a display panel. More particularly, the present invention relates to a method and apparatus for compensating propagation delay in display drivers through delaying a column driver enable signal by a time approximating the delay experienced by signals propagating in a corresponding row signal line. The present invention also relates to a method and apparatus for compensating propagation delay in display drivers through delaying a row driver enable signal by a time approximating the delay experienced by signals propagating in a corresponding column signal line.

2. Description of the Relevant Art: Many display panels, such as those used as televisions, computer monitors, and other video and stationary image displays, include a lattice of display signal lines formed in a plurality of rows and columns. Each junction of the lattice includes a switching device, typically a thin film transistor (TFT), a storage device, such as a capacitor, and an associated display element or pixel. To activate the switching devices to store the voltages necessary for appropriate pixels to display an image, column and row drivers are used in conjunction with one or more display controllers. The display controllers generate timing signals, such as column and row driver enable signals, for the respective column and row drivers which, in turn, generate appropriate voltage signals for specific pixel addresses. The use of pixels arranged in a lattice, as opposed to a cathode ray tube, enables relatively large display areas with relatively small display panel thickness.

The construction of a liquid crystal display (LCD) panel, for example, includes a plurality of addressed pixels formed in a lattice of pixel rows and columns. Each pixel in the lattice is addressed by a row selection signal line and a column driver signal line; a desired driving voltage is applied to such pixel, via the column driver signal line, when its row is selected via the row selection signal line. The aforementioned row selection signal line and column driver signal line are each coupled to control circuitry that determines what voltage will be applied to each pixel in a common row when that row is selected. In a color display panel, each position in the lattice preferably includes three subpixels for respectively emitting the primary colors red, green, and blue to provide a full color

display panel. During pixel addressing periods, individual row signal lines are selectively enabled to select one row of pixels at a time, and column signal lines of the LCD panel are selectively driven with voltages unique to the current image content of the LCD panel. Selective address voltages are generated by driver controllers that are specifically designed for direct coupling to the LCD panel row and column signal lines.

To refresh a display panel, a row enable signal is transmitted to a first row of display pixels. This row enable signal activates the transistors associated with each of the pixels on that row and enables the transistors to transfer voltages on the column signal lines to the capacitors associated with the relevant pixels in that row. Substantially simultaneous with the row enable signal activation, a select plurality of the column signal lines is activated and voltages are transferred to the appropriate capacitors. For color displays, each pixel is associated with three column signal lines (red, green and blue). The column signal line through which the voltage is transferred and the magnitude of that voltage determines what color an associated pixel will be, and with what intensity the color will display. After a predetermined time for transfer, the row enable signal is switched low, storing the transferred voltage value in the capacitor. After a delay, the process is then repeated for the next sequential row on the display panel until all rows have been refreshed.

Early display panels were manufactured to have a screen size on the order of 10" (diagonal measurement) with a pixel density of 640 x 480 pixels, and delay problems resulting from a signal traveling from circuitry at one end of the display to the circuitry at another end of the display were considered by many to be negligible. Over time, however, display panels have become larger and pixel density has increased. These changes in display panels have compounded the once minor delay problems to a point that they should no longer be considered negligible.

As an illustration of the significance of potential delay involved in a refresh cycle, a conventional QXGA display having 2,048 vertical columns and 1,536 horizontal rows of pixels will be discussed. For each vertical column of pixels in a color display, there are actually three vertical columns of storage devices for storing values, one each for red, green and blue. Therefore, in a color QXGA display, there are 6,146 columns and 1,536 rows of signal lines. Displays are conventionally completely refreshed at a rate of at least 60 times per second, or at 60 Hz, to avoid flicker. Other

displays, for example QSXGA+ displays, have even higher densities of pixels. With a QXGA color display having 1,536 rows of signal lines, the maximum time available to refresh each row (t_{Rmax}) is:

$$t_{R\max} = \frac{\left(\frac{1}{60s}\right)}{1536rows} = 10.85\mu s / row$$

For each additional row of pixels added to the display, the available time to refresh those pixels decreases. Furthermore, at points where display row and column signal lines cross, parasitic capacitance is observed between the conductive signal lines. This parasitic capacitance may further slow signal propagation. Conventionally, there is approximately a 1 to 2.5 microseconds delay in the row enable signal by the end of a signal line in a QXGA display. In other words, if the row enable signal applied at one end of the row enable line switches from low to high at time zero, then the low to high transition will not appear at the opposite end of the row enable line in anywhere from 1 to 2.5 microseconds later. Increasingly greater effort must be spent in the design of larger format display panels in order to maintain such propagation delays within reasonably small values. Practical factors currently limiting the state of the art dictate that such propagation delay be approximately 1 to 2.5 microseconds. Despite there only being approximately one-quarter the number of pixels in an XGA display as in a QXGA display, the row enable signal propagation delay of an XGA display is approximately the same as that observed in a QXGA display. As discussed in greater detail hereinafter, display signal propagation delay may cause noticeable uneven display intensity or even display errors.

In attempts to resolve what has previously been considered only a minor problem, others have used wider, less resistive, signal lines to increase signal propagation and decrease delay. However, as the physical dimensions of the signal lines are increased, the physical space available for use as pixels necessarily decreases; this results in decreased pixel size, or aperture, and hence, less display surface area for active light modulation. In turn, less active light modulation area results in more light source power for the same display brightness effect. Increasing the thickness of the address conductors reduces the resistance at the expense of fabrication time. Reducing the overlap capacitance between the row and column line conductors through thicker dielectric separation also

results in added fabrication expense. Other attempts at resolving the effects of display signal propagation delay include providing duplicate column drivers, one at the top of the display and one at the bottom of the display, and duplicate row drivers, one at the left of the display and one at the right of the display. Displays using these approaches, however, require additional circuitry and still may experience the varied pixel intensity problems caused by signal propagation delay.

Summary of the Invention

It is an object of the present invention to compensate for row signal propagation delays in a display panel.

It is a further object of the present invention to compensate for column signal propagation delays in a display panel.

It is a still further object of the present invention to delay row enable signals to approximate the propagation delay of corresponding column signals.

It is another object of the present invention to delay column enable signals to approximate the propagation delay of corresponding row enable signals.

It is yet another object of the present invention to generate delayed column enable signals having start times approximating the times a row enable signal will reach each column.

It is an object of the invention to generate delayed row enable signals having start times approximating the times a column signal will reach each row.

The present invention provides a method and apparatus for reducing the effects of signal propagation delay in a conventional display panel, such as an LCD panel. According to a first aspect of the present invention, the timing of a column driver enable signal is adjusted to approximate the propagation delay of a signal in a corresponding row signal line. By enabling the column signal lines with the delayed column driver enable signal, the negative effects of signal propagation delay are significantly reduced. A column driver circuit includes circuitry to delay a column driver enable signal, or other column timing signal, by an amount which approximates the delay of a row enable signal as it propagates to the column activated by the column signal.

According to a second aspect of the present invention, the timing of a row driver enable

signal is adjusted to approximate the propagation delay of a signal in a corresponding column signal line. By enabling the row signal lines with the delayed row driver enable signal, the negative effects of signal propagation delay are significantly reduced. A row driver circuit includes circuitry to delay a row enable signal, or other row timing signal, by an amount which approximates the delay of a column signal as it propagates to the row activated by the row enable signal.

Both digital and analog embodiments of display driver circuits are disclosed wherein a plurality of signal delay elements are operatively coupled together to delay a display timing signal propagating therethrough. The delay elements are chosen such that the delay experienced by a column or row timing signal approximates the delay experienced by a display signal propagating through a corresponding display line such as a row or column signal line.

Methods of compensating for display line signal propagation delay are also disclosed whereby a display line timing signal is generated. A first plurality of delayed display line timing signals is also generated and used to activate at least one row or column signal line. The first plurality of delayed display line timing signals is generated to approximate the delay of a signal propagating through an associated display line. A second plurality of delayed display line timing signals may also be generated in response to one or more of the first plurality of delayed display line timing signals to activate a display line of a display panel. In activating the display lines, the method may also track which display line is to be activated next, and select a delayed display line timing signal in accordance with an indication of the next display line to be activated. A method is also disclosed wherein a delayed display line timing signal is generated comprising components to activate a plurality of display lines at varying times from the timing signal components of the delayed display line timing signal. The components are each removed from the timing signal as they are used by a portion of the display driver circuit, and the remaining timing signal components are relayed to another portion of the display driver circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The nature of the present invention as well as specific embodiments of the present invention may be more clearly understood by reference to the following detailed description of the preferred

embodiment of the invention, and to the drawings herein, wherein:

Figure 1 is a block diagram of an LCD display panel configured according to a particular embodiment of the present invention;

Figure 2 is a timing diagram illustrating one effect of row enable signal propagation delay as between a column located near the row enable driver and a column located farther from the row driver;

Figure 3 is a timing diagram illustrating one effect of column signal propagation delay as between a row located near a column driver and a row located farther from the column driver;

Figure 4 is a graph illustrating several examples of delay/distance curves for row enable signal propagation delays;

Figure 5 is a diagram illustrating an analog implementation of a column driver enable signal delay circuit according to a particular embodiment of the present invention;

Figure 6 is a block diagram of a digital implementation of a column driver enable signal delay circuit according to an embodiment of the present invention;

Figure 7 is a diagram of a portion of a timing controller for a digital implementation of a column driver enable signal delay circuit according to an embodiment of the present invention;

Figure 8 is a timing diagram of the START and STOP signals generated by the column driver enable signal delay circuit shown in Figure 7;

Figure 9 is a circuit diagram of a digital implementation of a column driver circuit such as those shown in the block diagram of Figure 6 according to an embodiment of the present invention;

Figure 10 is a timing diagram of the individual column line enable signals at the output of a column driver enable delay circuit according to an embodiment of the present invention;

Figure 11 is a block diagram of a digital implementation of a row driver enable signal delay circuit according to an embodiment of the present invention; and

Figure 12 is a circuit diagram of one embodiment of a row counter circuit according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

To illustrate the specific nature of the signal propagation delay problem, reference is made to Figure 1. Figure 1 illustrates a portion of a display panel 2 having a plurality of row drivers 4 along the left side of the display and a plurality of column drivers 6 along the top of the display. Rows associated with the row drivers 4 are ordered sequentially from top to bottom and are conventionally refreshed in sequential order. The row drivers 4 and column drivers 6 are respectively controlled by row driver and column driver controllers 8 and 10 respectively. The row and column drivers 4 and 6 may be formed in common circuitry with the respective row and column driver controllers 8 and 10, or as separate circuitry. Row and column drivers 4 and 6 may be respectively placed along the right and bottom sides of the display in addition to or instead of the left and top sides, respectively.

When it is time to refresh the first row of pixels, a row enable signal is produced from the first row driver in the sequence of row drivers. In reference to Figure 2, when a row enable signal 20 goes high, the TFT transistors coupled to such row are turned on and the storage capacitors associated with such TFT transistors begin to charge to the voltage present on their associated columns; in Figure 2, column signals 22 and 24 represent two such columns located at opposite ends of the LCD display. Conventionally, the signals 22 and 24 on each of the column signal lines are activated at substantially the same time. As shown in the Near Column Signal Line example of Figure 2, for column signal lines nearer the row driver (e.g., column signal 22), the row enable signal 20 has little or no propagation delay and, therefore, is high at the near column for all or nearly all of the time the column signal 22 is activated. As shown in the Far Column Signal Line example, however, due to row enable signal propagation delay 26, the row enable signal 20 may not reach columns farther from the row drivers until after the corresponding column signal 24 has been activated. A portion of the charge 28 available through the column signal 24 falls within the time when the row enable signal 20 is high at that far column signal line and is, therefore, stored on an appropriate capacitor. The remaining portion of the charge 30, which ideally would have been available to help charge the appropriate capacitor, is missed due to the signal propagation delay 26. Furthermore, when the column signal 24 transitions low before the row enable signal 20 transitions low, the capacitor associated with the corresponding row and column address discharges until the

time row enable signal 20 transitions low, thus, further decreasing the charge on the capacitor from its appropriate charge value.

Because capacitors charge asymptotically and, therefore, never truly charge to their full value, the longer they charge, the closer to their full value they reach. Capacitors with full values stored are closer to their intended intensity than those with less than their full voltage value stored. The net effect of uncompensated propagation delay is that the pixels farther from the row drivers may be proportionately less or more intense than those pixels nearer the row drivers, or that the colors emitted by pixels nearer the row drivers do not match the colors emitted by pixels farther from the row drivers.

The explanation of the effects of column signal propagation delays is similar to that of the row signal propagation delays. In reference to Figure 3, every row is conventionally driven exactly the same length of time at a duration spaced evenly among the plurality of rows. The problem created by column signal propagation delay 42 is that it takes the column signal 34 longer to reach the pixel locations in the rows of the display farther from the column drivers than it takes for column signal 34 to reach those rows nearer the column drivers. As shown in the Near Row Signal Line example of Figure 3, row enable signal 38 may go high a significant time before the column signal 34 reaches the farthest rows of the display, and row enable signal 38 may go low again before the column signal charge 40 has been fully stored on the appropriate capacitor.

The present invention significantly reduces the effects of signal propagation delays by addressing row signal line propagation delay and/or column signal line propagation delay. While these two aspects of the present invention will be addressed separately below, it will be understood by those skilled in the art that these aspect of the invention may be implemented independently of each other or, more preferably, in a common display.

Row Enable Signal Propagation Delay Compensation

In regard to row signal propagation delays, the solution described herein involves a column driver circuit which generates column enable signals which are not simultaneously produced, but which are intentionally delayed by a circuit which approximates the propagation delay experienced by a row enable signal. These delayed column enable signals are then used to activate column signal

lines at a time where they will meet the propagation delayed row enable signals. In this way, each capacitor on a row is permitted to charge for approximately the same time regardless of its location along the row, and regardless of row enable signal propagation delays.

The present invention fairly approximates row propagation delays by using a stepwise linear approximation of a delay curve for a row enable signal propagation delay as a function of the row line length. Figure 4 includes a graph of three representative delay/distance curves 42, 44 and 46. A delay/distance curve may be charted by one of skill in the art by observing the actual propagation delay of a row enable signal in a display panel, or by simulating the circuitry of a display panel using one of the numerous electronics simulation software packages available on the market and plotting the timing signal of a row enable signal. An example of an appropriate electronics simulation software package is 'SPICE' distributed by Intusoft of San Pedro, California. The first curve 42 of Figure 4 will be used for the examples herein. Each display panel's circuit design and implementation will vary and involve a different curve. Once an appropriate delay/distance curve is generated, as described hereinafter, the particular delay circuitry may be selected and implemented to delay the signals by analog or digital circuitry.

Analog Implementation: One embodiment of the invention implemented as an analog circuit for delaying the column driver signals is illustrated in Figure 5. The lower portion 60 of Figure 5 represents a display panel including a lattice of rows and columns, pixels, capacitors and transistors. For a display panel, each pixel-capacitor-transistor-conductor combination in the lattice may fairly be modeled by a resistor and a capacitor to approximate the impedance and parasitic capacitance effects on a row enable signal. To create a delay for the column driver enable signal which approximates the delay experienced by a row enable signal, a plurality of resistive and capacitive elements 66 and 68 are coupled in a delay line as shown in Figure 5. The blocks CD1, CD2 . . . CD10 represent column driver circuits 70, 72, 74, 78 and 80 for groups of column signal lines in a display panel. The input node IN receives a conventional display timing signal for delaying by the delay circuit before sending it to the column driver circuits 70, 72, 74, 78 and 80.

To determine the values of resistors 66 and capacitors 68 needed in the delay line, the delay/distance curve selected for the particular display panel (see Figure 4 and related discussion)

may be analyzed to determine the resistor-capacitor combinations necessary to produce the desired delays. Numerous well known circuit modeling software packages, such as 'SPICE' distributed by Intusoft of San Pedro, California, are available commercially and may be of assistance in charting an appropriate delay/display curve and the required delay and/or resistive and capacitive components. The delay imposed on the column driver enable signal used for each column driver circuit 70-80 should be chosen to approximate the delay needed for the first column signal line among that group of column signal lines. As an example, by reference to the graph of Figure 4, if there are ten column driver chips CD1-CD10, the delay/distance curve would preferably be divided into 10 equally long sections 48. To approximate the delay of a row enable signal propagating across a display, the delay of the column enable signal needed at the input of a particular column driver circuit is the delay indicated by the graph at the beginning of that driver's group section 48. For the first curve 42 shown in Figure 4, the fourth column driver is sectioned between marks 52 and 54. The delay needed at the input to the fourth column driver CD4, therefore, is the delay corresponding to mark 52, or approximately 810 ns. The column driver enable signals for the fourth column driver CD4, therefore, are delayed 810 ns before entering the column driver for group 4. A larger or smaller number of groups and divisions may be formed as desired for a particular application.

As specifically illustrated in the fourth column driver block CD4 76 of Figure 5, in addition to conventional column driver circuitry, an embodiment of the present invention includes delay elements 82 to further delay the column enable signal for each individual column within that column signal line group. By further delaying the column enable signal, a more precise stepwise linear approximation 56 to the curve 42 is formed (*see* Figure 4). The necessary delay imposed by each delay element 82 may be determined by dividing the difference between the curve section for that column driver (e.g. 960 ns - 810 ns for CD4 between marks 52 and 54 on Figure 4) by the total number of columns associated with that column driver. In other words, for a particular column driver, each of the delay steps may be made equal for simplicity of driver delay line design.

For different displays, however, there are different characteristics which need to be matched for the display drivers to operate most effectively. This may require individually varying the values of each of the display elements 66 and 68 to find an optimal approximation and, therefore, does not

necessarily lend itself to easy adjustments. Furthermore, analog designs are notoriously susceptible to noise and other well known problems associated with analog systems in some applications. While the analog implementations described herein will reduce the effects of row signal propagation delay in display panels, it may be preferable in some cases to use a digital implementation of the invention.

Digital Implementation: As will be clear to one of ordinary skill in the art, the principles behind implementing the delays for display driver enable signals according to the embodiments of the invention in a digital system are similar to those behind implementing the delays in an analog system The same delay/distance curve and calculations may be used for either system, and will, therefore, not be rediscussed here.

For a digital implementation of the column enable signal delay circuitry according to an embodiment of the invention, reference is made to Figures 6-10. Figure 6 illustrates a general block diagram of the column enable signal delay circuitry 100 which includes a timing controller 102, a plurality of column driver circuits 104, 106, 108, 110 and 112, and START 114 and STOP 116 signal lines coupling each of the column driver circuits 104-112 together in series with the timing controller 102. Alternatively, the timing controller 102 could be directly wired to each of the column driver circuits 104-112. This approach, however, would require additional wiring and space.

Figure 7 illustrates one embodiment of a delay portion of the timing controller circuit shown in Figure 6. Instead of the resistors and capacitors used in the analog embodiment shown in Figure 5, this digital embodiment uses a delay locked loop 120 to create appropriate delays Δ_0, Δ_1, Δ_2 . . . Δ_{N-1} in the column enable signal or other display driver timing signal. By tapping the delay locked loop, at select locations which provide the necessary delay for the column enable signal, appropriately delayed column enable signals may be sent to each of the column driver circuits 104-112. Additionally, a calibration circuit 122a and 122b may be configured in a feedback loop for making automatic and selective adjustments to the timing of the delays created by the delay locked loop 120.

For automatic adjustments to the timing of the delays, feedback loop circuitry 122b is coupled to the individual delay elements of the delay locked loop 120 which uniformly adjusts the delay of every delay element in response to a comparison between the output of the delay locked

loop 120 and a reference signal at node 126. When a signal is detected at the input node IN 128 of the delay locked loop 120, a pulse is generated to activate a switch 62, which couples a first reference voltage, such as Vcc, across a variable impedance 124. A comparison between the discharge of the voltage on the variable impedance 124 and a voltage measured between two resistors 130 determines the reference signal at node 126.

For selective adjustments, by increasing the value of the variable resistor 136 in the variable impedance 124, the voltage on the capacitor 134 dissipates slower. By decreasing the value of the variable resistor 136, the voltage on the capacitor 134 dissipates more quickly. If the two resistors 130 are equal, the comparator 132 will be timed to adjust the delay locked loop delays to allow the column enable signal to reach the end of the delay locked loop 120 when the capacitor of the variable impedance 124 is half discharged. Other variable impedance elements may be substituted for the variable resistor 136 and fixed capacitor 134 shown in this embodiment. By using a delay locked loop 120 with a calibration circuit 122, the specific timing of the delay elements is more easily adjusted.

The appropriately delayed column enable signals are tapped by to two similar sets of circuitry: one circuitry 140 to generate a START signal, and one circuitry 142 to generate a STOP signal. The STOP signal is the same as the START signal, but delayed in time by the width of the column enable signal (τ_{CS} on Figure 8). The width of the column enable signal (τ_{CS}) may also be used to establish the parameters of a "charge share" feature known in the art and described in U.S. Patent No. 5,852,426, issued December 22, 1998, to Erhart, et al., and assigned to the assignee of the present invention, the disclosure of which is hereby incorporated herein by reference. As can be seen in the circuit of Figure 7, the circuitry 140 for the START signal includes a pulse generator 144, also called a mono-stable multivibrator or "one-shot", for each tap on the delay locked loop 120. The number of taps corresponds to the number of column driver circuits used. The pulse generators feed into an OR gate 146 which is coupled to a flip-flop circuit 148 clocked by the output of the OR gate 146. The only difference between the circuitry 140 to generate the START signal and the circuitry 142 to generate the STOP signal is that an inverter 150 is placed at the input of each pulse generator 144 for the circuitry 142 to generate the STOP signal. As shown in Figure 8, the effect of this

inverter is to initially clock the flip-flop 148 of the STOP circuitry 142 on the falling edge of the column enable signal rather than the rising edge.

As shown in Figure 6, the START and STOP signals are conducted to the first column driver 104. The first column driver 104 modifies the START and STOP signals and sends $START_1$ and $STOP_1$ signals to the second column driver 106. This process continues through the remainder of the column drivers. Figure 8 illustrates how the START, $START_1$, $START_2$ . . . and $START_{N-1}$ signals differ.

In reference to Figure 9, in addition to conventional column driver circuitry, each column driver circuit configured according to this embodiment of the present invention includes circuitry 160 to generate a delayed column driver enable signal for the column driver circuit, circuitry 162 to modify the START and STOP signals, and a delay locked loop circuit 164 with automatic calibration circuitry 166. The column driver circuits may be configured substantially identical to each other for simplification, or, in more sophisticated embodiments, the individual delay locked loops 164 within the column driver circuits may be adjusted to better approximate the specific segment of the delay/distance curve charted (*see* Figure 4 and related discussion).

When the START signal arrives at the first column driver CD1 104, the first rising edge 170 of the START signal (Figure 8), clocks the flip-flops 172 and 174 and initiates a column enable signal at the input of the delay locked loop 164. When the first rising edge 182 of the STOP signal (Figure 8) is received, it clocks flip-flop 176 and resets flip-flop 174 at the input to the delay locked loop 164. The first falling edge 184 and 186 of each of the START and STOP signals (Figure 8) is passed through respective first 178 and second 180 inverters, clocks a flip-flop 188 and activates an AND gate 190 to produce a rising edge at the output of the column driver stage. The first rising edge 170 and 182 of each of the START and STOP signals passing through a column driver stage is thereby stripped from the respective START and STOP signals and the signals are inverted before passing to the next successive column driver stage. Thus, the first rising edge passed to a column driver circuit corresponds to the timing delay needed for that column driver circuit to approximate the row signal propagation delay (Δ_0, Δ_1, Δ_2 . . . Δ_{N-1}) corresponding to that column driver's location on the display panel.

Within the delay locked loop 164, a tap or connection for each column signal line C_1, C_2 . . . C_M is made to the delay locked loop 164. The taps may be evenly spaced throughout the delay locked loop 164, or may be spaced to approximate the delay/distance curve charted (*see* Figure 4 and related discussion). If the delay locked loop taps are evenly spaced throughout the delay locked loop 164, the total delay for activation of a particular delayed column enable signal (Δ_{MT}), as compared to the activation time of the original column enable signal is represented by the following equation:

$$\Delta_{MT} = \Delta_{(j-1)} + \frac{2(M-1)+1}{2} * \frac{\Delta_j - \Delta_{(j-1)}}{M}$$

where j is the sequential number of the column driver, Δ_{j-1} is the delay for the START signal entering the column driver stage, Δ_j is the delay for the START signal leaving the column driver stage, and M is the sequential number of the column signal line in the column driver. Figure 10 shows a timing diagram for the individual column enable signals for the column signal lines within a particular column driver circuit with respect to the START and STOP signals at the input of the particular column driver circuit.

In summary, therefore, the purpose of the first delay locked loop 120 (Figure 7) is to establish the general delay times Δ_0, Δ_1, Δ_2 . . . Δ_{N-1} for the column driver circuits 104-112 (Figure 6) from the delay/distance curve (Figure 4). The purpose of the second delay locked loop 164 (Figure 9) is to establish the specific delay times for each of the column signal lines C_1, C_2 . . . G_M within each column driver circuit 104-112 (Figure 6).

<u>Column Signal Propagation Delay Compensation</u>

A row driver circuit operates similar to a shift register which steps through a sequence of rows, activating only one row at a time. The approach used to compensate a column signal propagation delay is similar to the previously described for row enable signal propagation delay. The approach involves generating a row timing signal which varies depending on the location on the panel of the present row being activated. As shown in Figure 11, a delay locked loop 200 is used to generate a plurality of delayed row timing signals for activating row enable signals. Row tracking circuitry 202 is used to evaluate which row or group of rows in the sequence of rows is presently

being activated. Finally, delay locked loop tap select circuitry 204 selects which delayed timing signal tap is appropriate for the present row being activated.

More specifically, when a row timing signal is received at the input to the timing delay circuit 206, it begins its process through the delay locked loop 200, is tapped by the tap select circuitry 204, such as a multiplexer switch, and clocks the row tracking circuitry 202. A row counter 208, such as a shift register, indicates to comparison circuitry 210 the count of the presently activated row. In the particular embodiment shown, digital comparators 212 within the comparison circuitry 210 compare the row counter indication with fixed count references 214. When the row counter indication exceeds a particular fixed count reference, the output of the digital comparator goes high. Based upon which of the outputs of the digital comparators 212 have most recently gone high, a priority encoder 216 sends an appropriate signal to the multiplexer switch 204 to adjust the delay tap from which the row clock signal is sent out. There are numerous other combinations of components which will operate equivalent to the circuitry described herein without departing from the basic principles and scope of the invention. For example, Figure 12 illustrates an embodiment of the row tracking circuitry 202 which receives a binary row count from the row counter 208 and uses a plurality of multiple input AND gates, each activated by different binary input combinations, to produce an input to a counter 218 which shifts each time a new group of rows has begun activation.

The specific row clock delay taps for the various groups of row signal lines chosen may be selected by comparison with a delay/distance curve for column signal delay propagation, or may be generally approximated if large delay groups are used. Alternatively, specific circuitry for each row signal line may be implemented, as was done with the column driver circuitry, to more precisely approximate the actual propagation delays experienced by column signals. Similarly, it will be understood by those of ordinary skill in the art that a less precise approximation of the row enable signal propagation delay will result in simpler circuitry for the column driver circuits. Various applications will necessitate varying levels of approximation precision and circuit complications. Furthermore, the circuitry for column signal propagation delay compensation according to embodiments of the present invention may alternatively be implemented in an analog configuration using the principles discussed previously herein.

Although the present invention has been shown and described with reference to particular preferred embodiments, various additions, deletions and modifications that are obvious to a person skilled in the art to which the invention pertains, even if not shown or specifically described herein, are deemed to lie within the scope of the invention as encompassed by the following claims.